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AF/2829/18

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Andoh	Docket No:	TI-31537
Serial No:	09/991,848	Examiner:	Hollington, Jermele
Filed:	37216	Art Unit:	2829
For:	NEW PEAK HOLD SCHEME		

EXTENSION OF TIME

Assistant Commissioner For Patents
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 1-15-04.

Tommie Chambers

Dear Sir:

Pursuant to 37 CFR 1.136(a), Applicant(s) respectfully petition(s) the Commissioner for an extension of the shortened statutory period for response in the above identified Application.

The fee for this extension is indicated below:

___	One Month ($110)	_X_	Three Months ($890)
___	Two Months ($390)	___	Four Months ($1,390)

Any further necessary extension of time is hereby requested. Charge any and all fees, or credit any overpayment, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in duplicate.**

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Applicant
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Andoh	Docket No:	TI-31537
Serial No:	09/991,848	Examiner:	Hollington, Jermele
Filed:	11/21/01	Art Unit:	2829
For:	NEW PEAK HOLD SCHEME		

APPEAL BRIEF PURSUANT TO 1.192(c)

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Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed June 3, 2003, and the Advisory Action mailed November 5, 2003.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1 and 2 were originally filed. Thus, the subject matter of the instant Appeal is the final rejection of Claims 1 and 2.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1 and 2. By virtue of an amendment filed on March 25, 2003, Claim 1 has been amended. An amendment after final was filed on August 18, 2003, amending no claims. The Advisory Action mailed November 5, 2003 indicated that the amendment filed on August 18, 2003 would be entered.

SUMMARY OF THE INVENTION

Turning to Figure 4, an input signal which may be the input signal of Figure 2 is input to a track and hold circuit 400 through input terminal 410. The hold circuit tracks the input signal and holds it and outputs an output signal in accordance with a clock signal which is input. The output of the track and hold circuit 400 is input to capacitor 406, and capacitor 406 is connected to the track and hold circuit 400 and connected to ground. Connected in parallel to the capacitor 406 is constant current source 404. The constant current source 404 is connected to the track and hold circuit 400 and connected in parallel to the capacitor 406. The capacitor 406 forms a voltage from the charge resulting from the output of the track and hold circuit 400 and produces a peak hold voltage as an output voltage. The output of the track and hold circuit 400 is connected to the minus input of comparator 408. Additionally, the input signal is connected to the plus input of comparator 408. The output of comparator 408 is a series of pulses and is input to the clock input of the track and hold circuit 400.

In operation, the input signal is input to the track and hold circuit 400 as well as the comparator 408. The output from the track and hold circuit which corresponds to the current or old peak old voltage is input to the comparator, and a comparison is made

within comparator 408 to compare the new peak with the old peak voltage. The comparator 408 produces an output pulse whenever the input signal is greater than the current or old peak voltage. This output from the comparator 408 is a series of pulses which is input to the clock input of the track and hold circuit 400. Thus, the track and hold circuit outputs the input voltage in accordance with the output of the comparator circuit 404. The peak hold voltage is formed on capacitor 406 and is held. During non-clock pulses, the voltage of capacitor 406 is discharged through current source 404. The present invention provides a high peak hold voltage for input amplitude as illustrated in Figure 5 with a small amount of dead region.

ISSUES

The issues on appeal are at first whether Claims 1 and 2 comply with the written description requirement; second whether Claims 1 and 2 are in compliance with § 112, second paragraph; and third whether Claims 1 and 2 are anticipated by Hancock.

GROUPING OF THE CLAIMS

Claim 1 is independently patentable.

ARGUMENTS

Claims 1-2 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

These rejections are respectively traversed.

The Examiner alleges that the track and hold circuit to input the clock signal is not clear.

Additionally, the Examiner alleges that the specification does not provide clear, full, concise and exact terms as what is supplying the clock signal to the input of the track and hold circuit. The Examiner further alleges that the specification does not provide full, clear, concise, and exact terms that the pulses of the comparator output are clock signals.

Notwithstanding the allegations of the Examiner, the Examiner's attention is directed to page 6, lines 2-5 of the instant specification. Here, the (track and) hold circuit tracks the input signal and holds it and outputs an output signal in accordance with a clock signal which is input.

Clearly the clock signal is input to the track and hold circuit since that is the only circuit being discussed in the sentence.

Next, the Examiner's attention is directed to page 6, lines 12-14 of the instant specification. Here, the specification states that the output of comparator 408 is a series of pulses and is input to the clock input of the track and hold circuit 400.

Clearly, this means that the output of comparator 408 is input to the clock input of the track and hold circuit 400.

This is confirmed by Figure 4.

Lastly, the Examiner's attention is directed to page 6, line 21 where the specification states that the output from the comparator 408 is a series of pulses which is input to the clock input of the track and hold circuit 400.

Clearly the output of the comparator 408 is a series of pulses. Equally clear is the fact that these series of pulses is input to the clock input of the track and hold circuit 400.

Clearly, Claims 1 and 2 comply with § 112 including the enablement requirement in that the claims include subject matter which is described in the specification in such a way to enable one of ordinary skill in the art to which it pertains or which is most clearly connected to make and use the invention.

Claims 1 and 2 were rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitted essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections.

This rejection is respectively traversed.

The Examiner alleges that the admitted structural cooperative relationships are the relationships between the input circuit and the comparator.

The Examiner alleges that the input circuit produces an input signal that is received by the track and hold circuit which holds the input signal and produces a peak signal.

However, Claim 1 clearly indicates that the input circuit inputs an input signal.

The comparator compares the input signal and the peak signal. This is sufficient cooperative relationship of the elements to satisfy § 112.

Claims 1 and 2 are in full compliance with § 112.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hancock.

It is respectfully submitted that Hancock does not disclose or suggest the presently claimed invention including the track and hold circuit to input the clock signal.

The output of comparators U2 and U3 are not input to element 110.

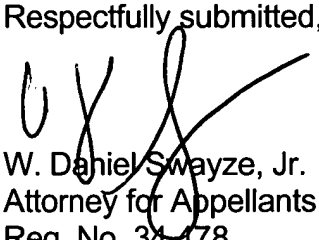
It is respectfully submitted that Claims 1-2 patentably define over the applied art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejections of Claims 1 and 2 under 35 U.S.C. § 112 and 35 U.S.C. § 102 are not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



W. Daniel Swayze, Jr.
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APPENDIX

1. A peak detector for detecting a peak signal, comprising:

an input circuit to input an input signal;

a track and hold circuit to hold said input signal and to output said peak signal;

a comparator to compare said input signal and said peak signal to generate a clock signal;

said track and hold circuit to input said clock signal and to output said peak signal in accordance with said clock signal.

2. A peak detector for detecting a peak signal as in Claim 1, wherein said peak detector includes a capacitor to hold said peak signal.

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